

CLAIMS

1. Security system for preventing unauthorized use, entrance or the like, comprising a number of secure devices<sup>(11)</sup>, each of said secure devices<sup>(11)</sup> comprising a chip with logic circuitry having a function in providing authorization to the security system, characterized in that in at least a <sup>(16)</sup>part of said secure devices<sup>(11)</sup>, the chip of a secure device<sup>(11)</sup> is provided with a unique chip layout.

2. Security system according to claim 1, wherein at least said logic circuitry<sup>(16)</sup> of the chips of said part of the secure devices<sup>(11)</sup> is implemented in FPGA technology, wherein the layout is programmed in the FPGA circuitry either in a volatile or non-volatile manner.

3. Security system according to claim 2, wherein the logic circuitry of each secure device chip is provided in a secure cell<sup>(15)</sup> of the chip.

4. Security system according to claim 1, wherein the complete secure device chip is implemented in FPGA technology, wherein the layout is programmed in the chip either in a volatile or non-volatile manner.

5. Security system according to claim 2, ~~3 or 4~~, wherein the logic circuitry or the entire chip is made as a volatile programmable FPGA, wherein the FPGA program is stored in a battery powered RAM.

6. A set of secure devices <sup>(11)</sup> ~~to be used in a security system according to anyone of claims 1-5~~, wherein each of said secure devices<sup>(11)</sup> comprises a chip with logic circuitry having a function in providing authorization to the holder of a secure device<sup>(11)</sup>, wherein in at least a <sup>(11)</sup>part of said secure devices<sup>(11)</sup>, the chip of each secure device is provided with a unique chip layout.

7. A set according to claim 6, wherein at least said logic circuitry of the chips of said part of the secure devices<sup>(11)</sup> is implemented in FPGA technology, wherein the layout is programmed in the FPGA circuitry either in a

volatile or non-volatile manner.

8. Method for manufacturing a secure device <sup>(11)</sup> for a security system according to ~~anyone of claims 1-5 or for a set of secure devices~~ <sup>chain</sup> according to claim 6 or 7, wherein <sup>(11)</sup> secure devices with a chip are used, said chips having logic circuitry having a function in providing authorization to the security system, wherein in at least <sup>groups</sup> ~~a part~~ of said secure devices, the chip of a secure device is <sup>manufactured</sup> ~~provided~~ with a unique chip layout.

9. Method according to claim 8, wherein chips with logic circuitry in FPGA technology are use, said method comprising the steps of programming a unique information <sup>(13)</sup> in the logic circuitry by means of synthesis tool <sup>(20)</sup> and a layout tool <sup>(22)</sup>, wherein for each secure device <sup>(11)</sup> of said part of secure devices <sup>(11)</sup>, a variation factor is introduced in at least one of the synthesis tool <sup>(20)</sup> and the layout tool <sup>(22)</sup>, thereby providing a unique circuit layout.

10. Method according to claim 9, wherein the synthesis tool <sup>(20)</sup> is provided with input information compiled from a high level language code <sup>(17,8)</sup>, wherein a variation factor <sup>(17)</sup> is introduced in at least one of the compilation step of the high level language code <sup>(17,8)</sup>, the synthesis tool <sup>(20)</sup> and the layout tool <sup>(22)</sup>.